CLAIMS

What is claimed is:

1. A computer system, comprising:

a processor having a power supply with a voltage;

a first circuit, coupled to the processor, that monitors the power supply voltage; and

a second circuit, coupled to the first circuit, that increases a clock period of a clock coupled to the processor over a predetermined number of clock cycles if the first circuit detects that the power supply voltage is less than a reference voltage.

2. The computer system of claim 1, wherein the second circuit decreases the clock period for a plurality of clock cycles after the increase in the clock period.

3. The computer system of claim 1, further comprising:

a phase locked loop (PLL), coupled to the second circuit, that generates the clock, wherein the clock is distributed to the processor.

4. The computer system of claim 1, wherein the computer system is a desktop computer.

5. The computer system of claim 1, wherein the computer system is a server.

6. A circuit, comprising:

a trigger control that adjusts the rise and fall time settings of a clock;

a first register coupled to the trigger control, wherein the first register

contains a default rise and fall settings of the clock, wherein the trigger control uses the rise and fall settings to adjust the clock; and

m registers coupled to the first register, wherein m is an integer greater than or equal to one, wherein each of the m registers has rise and fall settings that increase a period of the clock, wherein the trigger control accesses the m registers if a power supply voltage is detected to be less than a reference voltage.

7. The circuit of claim 6, further comprising:

n registers coupled to the m registers, wherein n is an integer great than two, wherein the n registers have rise and fall settings that allow the clock to recover the period increases from the m registers.

8. The circuit of claim 7, wherein the total decrease in clock period caused by the rise and fall settings of the n registers is less than a frequency guard band.

9. The circuit of claim 7, wherein the m registers and the n registers are preset via fuses.

10. The circuit of claim 7, wherein the m registers and the n registers are preset via metal options.

11. The circuit of claim 7, wherein the m registers and the n registers are revised via a TAP controller.

12. The circuit of claim 7, wherein the m registers and the n registers are revised via a microprocessor status register.

13. The circuit of claim 7, wherein the m registers and the n registers are revised

via a processor abstract layer.

14. The circuit of claim 6, further comprising:

a clock edge control buffer coupled to the trigger control, wherein the clock edge control buffer uses the rise and fall settings provided by the trigger control to independently adjust the clock rise and fall edge timings.

15. A clock modulation circuit, comprising:

means for detecting a power supply voltage droop; and

means for stretching a clock period after detecting the voltage droop.

16. The clock modulation circuit of claim 15, further comprising:

means for programming the clock period stretch.

17. The clock modulation circuit of claim 15, further comprising:

means for recovering the clock period stretch.

18. A method, comprising:

detecting a droop in a power supply voltage;

generating a droop trigger;

accessing the rise and fall delay values from a plurality of registers; and

adjusting the rise and fall edge delays of the clock.

19. The method of claim 18, further comprising:

programming the plurality of registers with rise and fall delay values.

20. The method of claim 18, wherein adjusting the rise and fall edge delays of the clock comprises stretching the clock period.

21. The method of claim 20, wherein adjusting the rise and fall edge delays of

the clock comprises recovering delays added to the clock during stretching of the clock period.

22. The method, comprising:

monitoring a voltage applied to a processor;

increasing the period of a clock applied to the processor if the voltage drops below a predetermined potential; and

decreasing the period of the clock to compensate for the increase in clock periods.

23. The method of claim 22, wherein the clock period is decreased to the original clock frequency of the processor prior to the voltage drop.